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10/669,095	09/23/2003	Michael R. Butts	706316-1224	1861

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EXAMINER

ROSSOSHEK, YELENA

ART UNIT PAPER NUMBER

2825

DATE MAILED: 10/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary**Application No.**

10/669,095

Applicant(s)

BUTTS, MICHAEL R.

Examiner

Helen Rossoshek

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 August 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 8-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 8-11, 14-17, 19, 20 is/are rejected.
- 7) ☒ Claim(s) 12, 13, 18, 21 and 22 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to the Application 10/669,095 filed 09/23/2003 and amendment filed 08/18/2006.

2. Claims 8-22 remain pending in the Application. Claims 1-7 and 23 have been cancelled from the Application.

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/18/2006 has been entered.

4. Applicant's arguments have been fully considered but they are not persuasive.

Claim Objections

5. Claims 8 and 17 are objected to because current amendment does not clarify amended limitation, but makes it more vague. First, it is not clear the meaning of the term "at least one programmable logic" (is word "device" missed?). Secondly, amended limitation leaves the question open: what was programmed (processor or programmable logic device) to simulate what.

6. Claim 18 is objected to because of the following informalities:

Claim 18 line 4 after "to" delete "the" insert --a--

Claim 18 line 5 after "to" delete "the" insert --a--

Claim 18 line 6 after "to" delete "the" insert --a--

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 8-11, 14-17, 19, 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Hoare et al. (US Patent Application Publication 20020133325).

With respect to claim 8 Hoare et al. teaches a method for implementing a design verification system into at least one programmable logic device so that a user design to be verified can be implemented therein within the method and system for the functional verification of the circuit design (abstract; paragraph [0103]), comprising: mapping the user design into operations for execution (within a central scheduler to evaluate discrete events including discrete event simulation engines (processor types) including mapping different types of simulation engines (processor types) to multiple components of the discrete event system (paragraphs [0065], [0034], [0067], paragraphs [0037]-[0041])); partitioning each of the operations into processor types suitable for each of the operations (within dividing the netlist into subgroups of components based on the type of the simulation engine that will be used to evaluate the component (paragraph [0067])); ordering each of the processor types according to connectivity of each of the

processor types (within the central scheduler to sort and schedule executing discrete events sequentially (paragraph [0034])); scheduling communications between each of the processor types within direct input and output queues between the scheduler and each of the simulation engines (paragraph [0035]); and programming the processor types into the at least one programmable logic device such that the at least one programmable logic is programmed to implement the processor types (within the system containing processors that are programmed for simulation (paragraphs [0029], [0097]), wherein a reprogrammable core-processor is one of the parts of the simulation engine (claim 2 of Hoare et al.).

With respect to claim 17 Hoare et al. teaches a method for verifying functionality of an electronic design within the method and system for the functional verification of the circuit design (abstract; paragraph [0103]), the electronic design including Boolean logic gates, at least one macro function and at least one memory circuit as shown on the Fig. 6 (abstract; paragraph [0108]), comprising; compiling the electronic design into logic processors that execute the Boolean logic gates (abstract), at least one macro processor that executes the at least one macro function, at least one memory processor that executes the at least one memory circuit as shown on the Fig. 6 one of the three simulation engine such as macro block (logic) engine (paragraphs [0108], [0111]), wherein macro block (logic) engine includes logic memory for execution instructions (paragraph [0032]) and there might be multiple engines of the same type, such as two different primitives and macro block engines (paragraphs [0108], [0041]); and an interconnect architecture that interconnects the logic processors, the at least one macro

processor and the at least one memory processor to one another as shown on the Fig. 6 as combination of the multiple simulation engines, wherein the combination might be in different various (paragraphs [0041]; [0108]); programming the logic processors, the at least one macro processor and the at least one memory processor into at least one programmable logic device such that the at least one programmable logic is programmed to implement the logic processors, the at least one macro processor and the at least one memory processor hardware (within the system containing processors that are programmed for simulation (paragraphs [0029], [0097], wherein a **reprogrammable core-processor** is one of the parts of the simulation engine (claim 2 of Hoare et al.) wherein each simulation engine comprising **reprogrammable core-processor** comprises a logic simulation, memory simulation etc. (claims 3-6 of Hoare et al.)); applying stimulus to the logic processors programmed into the at least one programmable logic device, the at least one macro processor programmed into the at least one programmable logic device and the at least one memory processor programmed into the at least one programmable logic device such that the logic processors execute the Boolean logic gates, the at least one macro processor executes the at least one macro function and the at least one memory processor executes the at least one memory circuit within hardware accelerators (processors) (paragraph [0097]) which utilize FPGAs (paragraph [0102]) as shown on the Fig. 6 one of the three simulation engine such as macro block (logic) engine (paragraphs [0108], [0111]), wherein the Boolean instruction is one of the plurality events might be simulated (abstract), wherein macro block (logic) engine includes logic memory for execution

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instructions (paragraph [0032]) and there might be multiple engines of the same type, such as two different primitives and macro block engines (paragraphs [0108], [0041]); and collecting output responses generated by the logic processors programmed into the at least one programmable logic device, the at least one macro processor programmed into the at least one programmable logic device and the at least one memory processor programmed into the at least one programmable logic device within the method and system for verifying the integrated circuit design using hardware emulator (accelerator), which utilize FPGA, wherein FPGAs enable processor-based (hardware) emulator as described above, including the scheduler and simulation engines for collecting the results of the verification process (abstract; paragraph [0069]).

With respect to claims 9-11, 14-16, 19, 20 Hoare et al. teaches:

Claim 9: the processor types comprise logic processors, macro processors, memory processors and general-purpose processors (within different types of simulation engines (paragraphs [0031], [0097]), wherein each simulation engine comprising reprogrammable core-processor comprises a logic simulation, memory simulation etc. (claims 2-6 of Hoare et al.));

Claims 10, 19: at least one memory processor comprises: an instruction memory (within second simulation engine as a memory simulation engine (paragraphs [0032], [0112])); a memory functional unit that can store data (paragraph [0112]); a register file controlled by the instruction memory, the register file having outputs selectively in communication the memory functional unit, the register file comprised of input registers and local registers, the input registers in communication with the interconnect

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architecture, the local registers in communication with output from the memory functional unit (paragraphs [0170]-[0172], Figure 8);

Claims 11, 20: a general purpose processor, the general purpose processor comprising a central processing unit that executes computer instructions, the general purpose processor in communication with the at least one logic processor and the at least one macro processor through the interconnect architecture (paragraph [0031]);

Claim 14: the partitioning step comprises: consulting a programmable logic device library that has a preprogrammed mix of said processor types within dividing the netlist into subgroups of components based on the type of the simulation engine that will be used to evaluate the component (paragraph [0067]); and selecting an appropriate preprogrammed mix of said processor types for said operations for execution within the central scheduler to sort and schedule executing discrete events sequentially (paragraph [0034]) including direct input and output queues between the scheduler and each of the simulation engines (Paragraph [0035]);

Claim 15: scheduling step comprises: creating a program for instruction memories within each of said processor types as shown on the Fig. 3 (paragraph [0079]); and creating programming files for each programmable logic device used for verifying the user design (paragraphs [0084], [0085]);

Claim 16: loading the program into each of the instruction memories (paragraph [0085]).

Allowable Subject Matter

9. Claims 12, 13, 18, 21, 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not disclose the specific arrangement of elements including logic processors comprising: an instruction memory; a logic functional unit that executes Boolean logic instructions; and a register file controlled by the instruction memory, the register file having outputs selectively in communication with the logic functional unit, the register file comprised of input registers and local registers, the local registers in communication with output from the logic functional unit (claims 12, 21); similar steps as disclosed in the limitations of the claims 13 and 22; the interconnect architecture comprising: an instruction memory; a plurality of buffers, wherein the number of the plurality buffers is equal to a sum of the number of the logic processors added to a number of the at least one macro processor added to a number of at least one memory processor, each of the plurality of buffers having an output that is selected by the instruction memory; plurality of selectors, wherein the number of the plurality of selectors is equal to the number of the plurality of buffers, each of the plurality of selectors in communication with each of the plurality of buffers so that data stored in any of the plurality of buffers can be transmitted to any of the plurality of selectors, each of the plurality of selectors controlled by the instruction memory; and plurality of output ports, each of the plurality of output ports corresponding to one of the plurality of selectors (claim 18, after overcoming aforementioned objections).

Remarks

10. In the remarks Applicant argues in substance:

a) nowhere does Hoare disclose, teach or suggest programming the processors of the simulation engines into a programmable logic device such that the programmable logic device is programmed to implement the processors of the simulation engines

8. Examiner respectfully disagrees for the following reasons:

As to a) Hoare et al. discloses a computer-based simulator capable of simulating many different event-based scenarios, such as a discrete event simulator that computes any scenarios (paragraph [0031]), wherein computer-based simulator comprises one or more simulation engines, such as logic simulation engine (paragraph [0111]), memory simulation engine (paragraph [0112]), behavioral simulation engine (paragraph [0115]), interconnection simulation engine (paragraph [0117]) as shown on the Fig.6 (paragraph [0108]). Moreover Hoare et al. discloses the system containing processors that are programmed for simulation of the integrated circuit design (paragraphs [0029], [0097]), wherein a **reprogrammable core-processor** is one of the parts of the **plurality of simulation engines/processor types** (claims 2-6 of Hoare et al.).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen.Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PAUL DINH
PRIMARY EXAMINER

A handwritten signature in black ink that reads "Paul Dinh". The signature is written in a cursive, flowing style with a long horizontal stroke extending to the right.

Helen Rossoshek
Examiner
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